

Study of Carbon Nanotubes as Etching Masks and Related Applications in the Surface Modification of GaAs-based Light-Emitting Diodes

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Nanostructures based on metals or semiconductors are proven to show excellent performance in the electro-optics field, especially when the feature size of the nanostructures is decreased to the wavelength of visible light.^[1,2] To fabricate the nanostructures, electron beam lithography (EBL), focused ion beam (FIB), and related etching methods are typically adopted, because the resolution and precision of the structures can be ensured with top-down methods on the scale of tens of nanometers.^[3,4] However, the application of EBL and FIB is greatly limited by the high cost and relative low efficiency.

Alternatively, nanomaterials such as polystyrene nanospheres^[5,6] and anodic aluminum oxide^[7] have been employed as etching masks for large area nanostructure fabrication. However, the morphology and distribution of these fabricated structures are restricted to the spherical shape of these nanomaterials. Furthermore, such materials are assembled by a self-organized process, in which a solution environment and subsequent processing steps are required. This method is usually not compatible with current semiconductor fabrication processes.

Nanoscale surface modification has been studied to enhance output light power of gallium nitride (GaN) and gallium arsenide (GaAs) based light-emitting diode (LED) devices.^[8–10] Since in these materials, the light extraction efficiency is limited by several factors, including the high refractive index of *p*-GaAs (approximately 3.3). The high refractive index leads to a low angle of total internal reflection (TIR) at

each boundary in conventional planar LED devices. Electron beam lithography and holography, combined with inductively coupled plasma-enhanced reactive ion etching (ICP-RIE), have been used to fabricate nanostructures on the surfaces of LED devices based on GaN and GaAs materials. Other approaches utilizing photonic crystals^[11,12] and metal oxide nanoparticles^[13–16] have also been explored to enhance the optical performance of III–V compound devices. These techniques are effective in the field of light extraction, but they cannot be used in the LED fabrication industry due to the high costs and low efficiencies during mass production.

In this research, we report a simple method for nanostructure fabrication using super-aligned multiwalled carbon nanotube (SACNT) thin films as etching masks for top-down etching processes. The morphology of the carbon nanotube (CNT) networks can be transferred to the substrate material at the macro scale, as the SACNT films may be fabricated conveniently over an area of square inches. Nanostructures on the scale of 100 nm were fabricated for the first time under a mask defined by SACNT networks. With this method, the nanostructured SACNT network morphology significantly increases the optical output power of GaAs devices in comparison with planar GaAs LED devices.

As a macroscopic material system that could be put into mass production at low costs, the super aligned multi-wall carbon nanotube networks have proved their excellent performance in electrical, optical, and mechanical properties.^[17–19] Carbon nanotubes have also been proven to be effective in the fabrication of microscopic mask structures.^[20] However, applications are restricted because pure CNTs are not durable in the RIE process. For the purposes of GaAs surface texturing, the morphology of SACNT network is one of the best options due to the appropriate length scale and quasi-periodic, directional characteristics. GaAs patterned with SACNT network were fabricated following the sequence depicted in **Figure 1**. The SACNT film was pulled out from CNT arrays^[17] and fixed on a metal frame in a cross-stacked manner. Al₂O₃ with a thickness of 10 nm was deposited by e-beam deposition on the suspended SACNT films. Next, the networks were transferred to GaAs substrate, on top of which 10 nm of SiO₂ was previously deposited. During the transfer process, alcohol was dropped on the Al₂O₃-SACNT film after it was placed on the GaAs substrate. The alcohol shrinks the

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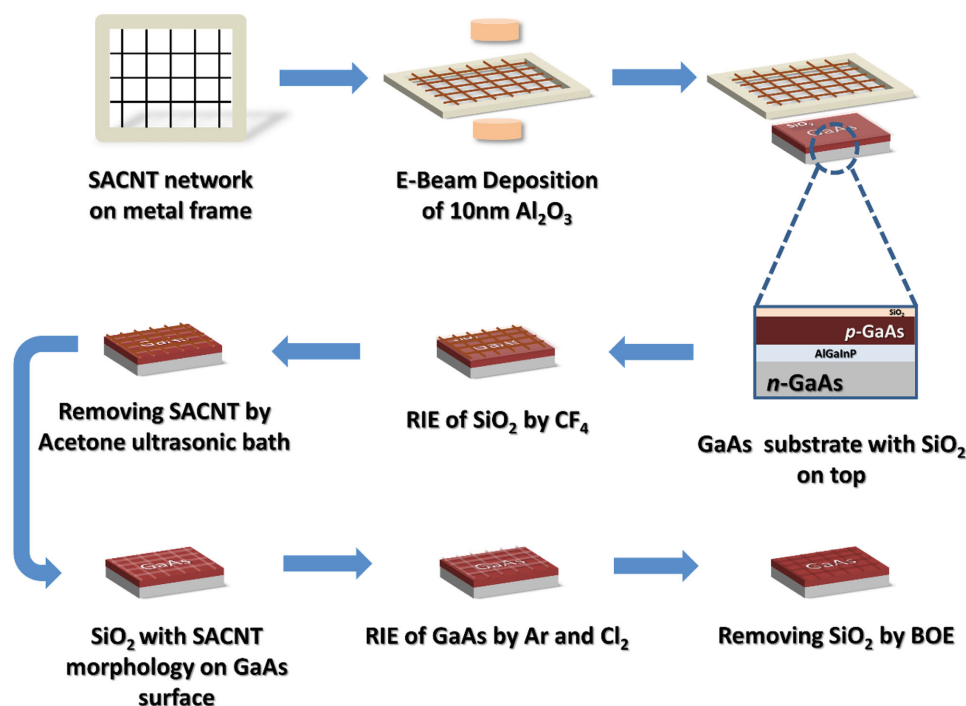


Figure 1. Schematic illustration of the fabrication process for patterning GaAs substrates with nanostructured, SACNT network morphology.

carbon nanotubes so that the film could be combined with the substrate more closely. The SiO_2 layer on the GaAs was employed as an intermediate in the RIE process. After the RIE process with CF_4 plasma (40 sccm, 2 Pa, 40 w, 20 s), the morphology of the SACNT network was transferred to the 10 nm SiO_2 layer. After removing the SACNT networks in an acetone ultrasonic bath, the GaAs was etched by Ar and Cl_2 (Ar for 10 sccm and Cl_2 for 25 sccm, 10 Pa, 50 w) under the SACNT-patterned SiO_2 mask. Finally, the SiO_2 mask was etched away with a buffered oxide etch (BOE) solution, leaving only the GaAs surface patterned with the SACNT network morphology. After surface modification, the patterned GaAs was used to fabricate an LED with a mesa area of 1 mm^2 . A transparent conducting layer (TCL) of Cr (2 nm)/Au (5 nm) was deposited on the *p*-GaAs surface. Cr (5 nm)/Au (100 nm) electrodes were then fabricated by photolithography and electron-beam evaporation on the *n*-GaAs layer and TCL as *n*- and *p*-pads, respectively. For comparison, a standard planar LED device was fabricated with a TCL directly deposited on the *p*-GaAs layer surface. All other fabrication processes were the same as those used for the SACNT-patterned LED devices.

The SACNT thin film was directly extracted from CNT arrays composed of aligned CNTs with diameters of approximately 20 nm. This method is convenient for mass production of SACNT films at low cost. An scanning electron microscope (SEM) image of the cross-stacked SACNT networks is shown in Figure 2a. The SACNT network was suspended on the metal frame such that the CNTs could be better surrounded by the deposited oxides in the subsequent e-beam evaporation processes. Figure 2b shows a transmission electron microscopy (TEM) image of carbon nanotubes with a 10 nm deposited layer of Al_2O_3 . As can be seen, the carbon

nanotubes in SACNT network have been totally surrounded by 10 nm Al_2O_3 thin film. No carbon nanotubes are exposed, thus guaranteeing the network to be good mask in the RIE process. This is crucial for the patterning process since carbon materials can be easily etched by most etching gases during plasma bombardment. The 10 nm Al_2O_3 thin film is the minimum thickness possible because thinner Al_2O_3 films do not completely shield the CNTs. Al_2O_3 thin films thicker than 10 nm would reduce the etching resolution.

Figure 2c shows the surface morphology of GaAs substrates after etching with Ar and Cl_2 plasma for 50 s. It can be seen that the SACNT morphology has been completely transferred to the surface of the GaAs substrate. Compared with the SACNT networks, the obtained pattern on the GaAs surface appears smooth and tidy, while the SACNT film appears more rough. As shown in Figure 2d, after the etching process, nanowires in the shape of CNTs formed on the surface of the GaAs. However, unlike how the CNTs are stacked at cross junctions, the nanowires on the surface of the GaAs are in the same plane at all junctions. The widths of the fabricated GaAs nanowires are 100 nm, and depend on the width of the masking CNTs. Considering that the average thickness of the SACNT thin film is 40–80 nm, the average width of each CNT bundle is several tens nanometers. With the addition of the 10 nm Al_2O_3 coating on the CNTs, the resolution of this etching method could easily reach 100 nm. The resolution can be further improved by decreasing the thickness of the SACNT thin film.

The atomic force microscopy (AFM) image of the nanostructured GaAs surface patterned with the SACNT network morphology is shown in Figure 3a. It is observed that the nanostructured GaAs surface morphology is uniform, since the nanowires share similar heights. The height of

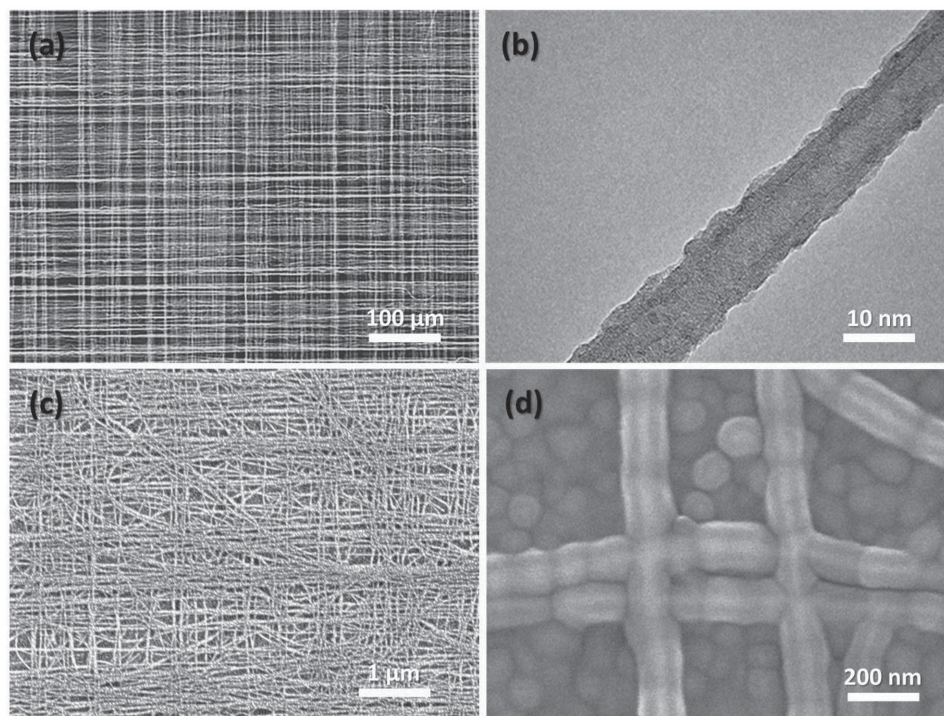


Figure 2. Morphology of a SACNT thin film and the surface of GaAs after being etched. a) SEM image of the cross stacked SACNT films. b) TEM image of CNTs deposited with a 10 nm thin film of Al_2O_3 . c) SEM image of the etched GaAs surface patterned with the SACNT networks. d) Magnified SEM image of the etched GaAs surface, showing the detail of the GaAs nanowire junctions.

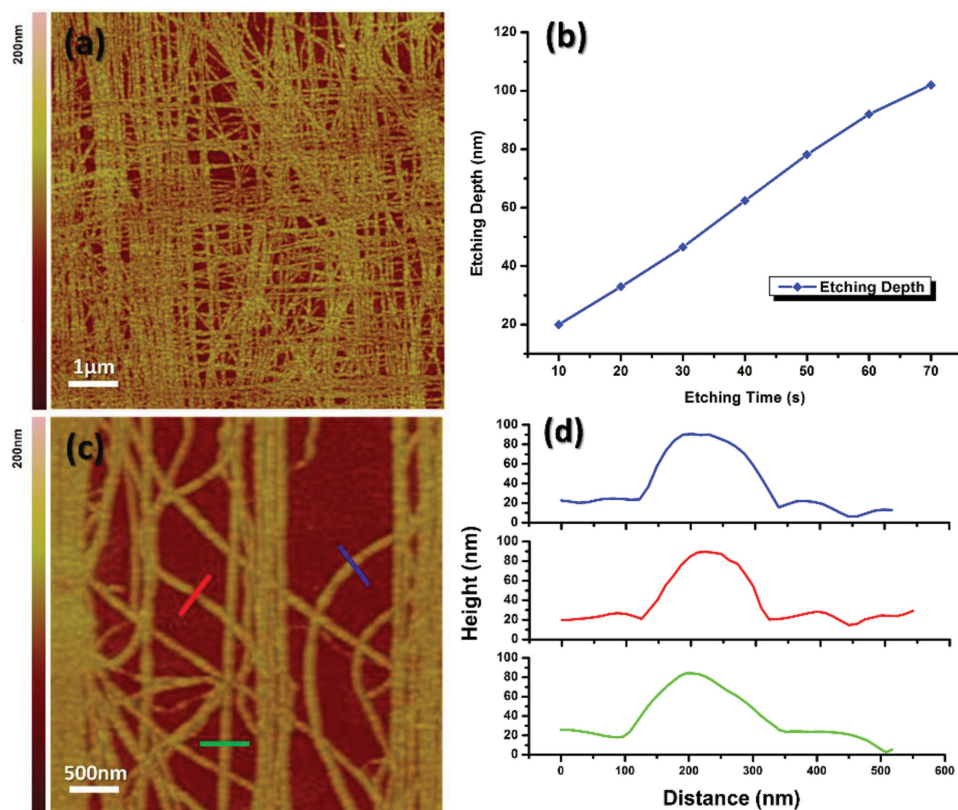


Figure 3. a) AFM image of a GaAs surface patterned with SACNT networks. b) GaAs etching depth as a function of etching time under Ar and Cl_2 plasma conditions. c) Local AFM image of a GaAs surface, and d) height comparisons among three random points on a patterned surface.

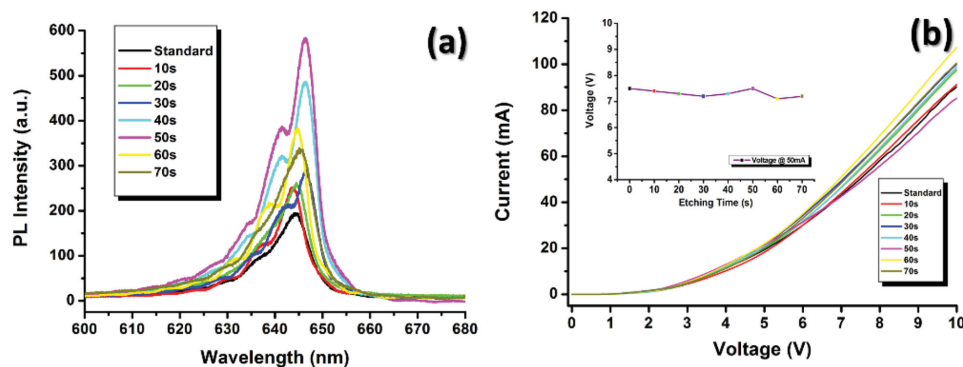


Figure 4. a) Room temperature photoluminescence spectra of GaAs LEDs with surface nanostructures fabricated at different etching times. A standard LED with a planar surface was used as a reference. b) I - V characteristics of samples fabricated with various etching times. The inset shows that almost all devices exhibit similar voltage performance under the drive current of 50 mA.

as-fabricated nanowires can be controlled by etching time under the masking of patterned SiO_2 , as shown in Figure 3b. At etching times less than 50 s, the height of the nanowires is proportional to the etching time. At etching times greater than 50 s, the etching rate is reduced, probably caused by the barrier effect of the already-formed GaAs nanowires. When a nanowire etched on the surface, plasma cannot penetrate as effectively as a pristine GaAs substrate. A magnified portion of the AFM image in Figure 3a is shown in Figure 3c so as to observe the structures more clearly. Three points on the AFM image were chosen randomly to measure the heights of the nanowires, which are shown in Figure 3d. At etching times up to 50 s, nearly all fabricated nanowires exhibit a height of 80 nm. This result demonstrates that the CNT/ Al_2O_3 composite etching mask and the SiO_2 intermediate layer were completely removed, and the nanostructures on the GaAs surface are comprised only of GaAs.

To evaluate the optical properties of as-fabricated GaAs LEDs, photoluminescence (PL) spectra were collected at room temperature. All samples were pumped at normal incidence angle by light from a semiconductor laser source ($\lambda = 514$ nm) with an excitation laser power of 10 mW. The laser passes through an attenuator and is focused onto the sample from the top side using a 50 \times objective lens with a focused spot diameter of 5 μm . As shown in **Figure 4a**, the PL intensity of the devices increases with etching time before the etching limit of 50 s. By comparing the PL spectra of the LED device with a standard device at an etching time 50 s, a maximum intensity enhancement of 2.97 \times of the PL peak is observed. For devices fabricated with etching times less than 50 s, the PL intensities were also increased compared to the standard planar device. These results should be attributed to the enhancement of light extraction efficiency obtained by surface patterning of GaAs. In the standard planar device, the light extraction efficiency is greatly limited by the total internal reflection at the interface of GaAs and air caused by the high refractive index of GaAs. After the GaAs surface was patterned with the SACNT network morphology, the total internal reflection condition changed as light excited more of the GaAs surface.

It should be noted that upon increasing the etching time from 50 to 60 s, the PL peak intensities decrease. Currently, it is widely accepted that by increasing the surface roughness or

by fabricating photon crystal structures on the surface of the LED devices, the TIR condition at the air–GaAs interface can be modified such that some guided modes of light can be extracted to increase the light extraction efficiency.^[4] With increasing nanostructure height, the critical angle at the air–GaAs interface increased as more light could be extracted from the device. However, for the very tall nanowires fabricated by etching times of 60 and 70 s, the emitted light can be significantly absorbed and reflected by the sidewalls of the nanowires, and thus causes the PL intensities to decrease. Furthermore, corresponding surface defects and materials damage induced due to prolonged RIE treatment would also have negative effect on the device performance.

The relationship between current and applied voltage of the GaAs LED devices are shown in Figure 4b. Nearly all of the GaAs LED devices with the SACNT network morphology, as well as standard planar sample, have the same I - V characteristics. In inset of Figure 4b, the voltage at an injection current of 50 mA was compared for all LED samples. At 50 mA, the device was operating under normal working conditions for a LED device driven by current. The corresponding voltages reached 7.5 V for all devices. These results indicate that the electrical properties of GaAs LED devices have not degraded by surface modification with SACNT network patterning.

Electroluminescence (EL) spectroscopy experiments were performed for all devices. The EL spectra were measured from the top side of the samples with a forward injection current of 50 mA at room temperature. **Figure 5a** shows that all devices, with and without the SACNT network morphology, exhibit a similar spectral peak at 647 nm and nearly the same full-width at half-maximum of 10–12 nm. This feature demonstrates that the SACNT network morphology surface modification does not damage the GaAs-based LED structure. For the device fabricated with an etching time of 50 s, the EL intensity was enhanced by 78% when compared with the standard, planar LED device. In our EL spectra counting, the peak intensity of LEDs etched for 50 s is 71.02, while the peak intensity for a standard device is 40.02. For devices fabricated by etching times of 10, 20, 30, and 40 s, the enhancement factors were 10.2%, 22.5%, 35.1%, and 40.1%, respectively. By further increasing the etching time to 60 and 70 s, the intensity of EL spectra decreased compared with the

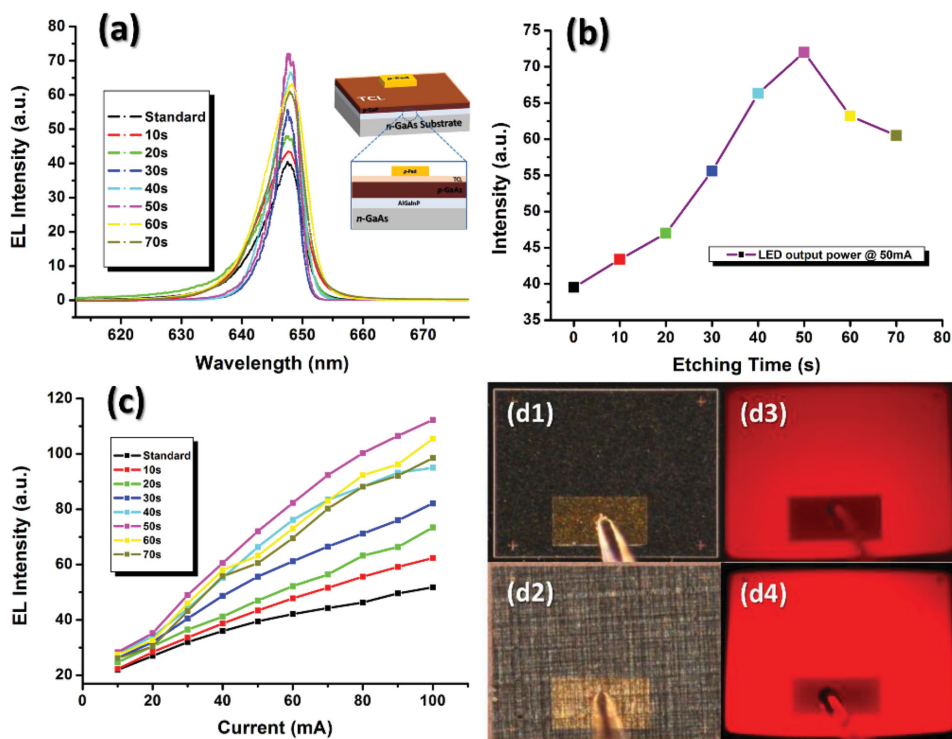


Figure 5. a) EL spectra of GaAs LEDs with nanostructured surfaces. Inset: cross-section schematic of the as-fabricated LED device structure. b) The EL intensities as a function of etching time at an injection current of 50 mA. c) Optical output power as a function of injection current for nanostructures fabricated at different etching times compared with a planar LED. d) Optical microscopy images of LEDs d1) without and d2) with nanostructured surfaces. d3, d4) Optical images of the corresponding lit devices at an injection current of 50 mA.

device etched for 50 s. The EL intensities of all LED devices measured with an injection current of 50 mA are listed in Figure 5b. The EL intensity behavior of these devices is consistent with their PL intensity performance.

Figure 5c shows the optical output power versus injection current (L - I) characteristics of all LEDs with and without SACNT network patterning on p -GaAs surfaces. For all devices, the output power first increases and then begins to saturate with increasing current. Optical microscopy images of the LED devices fabricated with SACNT network nanostructures at an etching time 50 s are shown in Figure 5d2, and may be directly compared with the standard LED sample shown in Figure 5d1. The nanostructures patterned by the SACNT network can be clearly observed on the surface of the devices. At an injection current of 50 mA, these two samples emitted light, as shown in Figure 5d3, d4, respectively. These results demonstrate how light extraction efficiency in GaAs LED devices can be improved by modifying the surface morphology with SACNT networks. Meanwhile, the fabrication technology is simple and practical. The SACNT networks can be produced efficiently such that this technology can be applied in mass production.

In conclusion, nanostructures on 100 nm scale were fabricated on GaAs surfaces using SACNT networks as a large-area, low-cost etching mask. The optical output power of LED devices based on patterned GaAs was enhanced by as much as 78% at an input current of 50 mA. These results were attributed to the surface modification of the GaAs material. Because the SACNT could be prepared in a suspended

manner, various types of masking materials may be chosen based on the etched material and etching process, making this method useful across a wide range of applications. This method has been shown to yield high quality nanostructures from super aligned carbon nanotubes, but should not be confined only to carbon materials, and could be extended to various other types of nanomaterials.

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- [1] S. Shoaee, J. Briscoe, J. R. Durrant, S. Dunn, *Adv. Mater.* **2014**, *26*, 263.
- [2] L. Vigderman, B. P. Khanal, E. R. Zubarev, *Adv. Mater.* **2012**, *24*, 4811.
- [3] G. Mariani, P. Wong, A. M. Katzenmeyer, F. Léonard, J. Shapiro, D. L. Huffaker, *Nano Lett.* **2011**, *11*, 2490.
- [4] J. J. Wierer, A. David, M. M. Megens, *Nat. Photonics* **2009**, *3*, 163.
- [5] J. Li, S. K. Cushing, P. Zheng, F. Meng, D. Chu, N. Wu, *Nat. Commun.* **2013**, *4*, 2651.
- [6] L. Ji, Y. Chang, B. Fowler, Y. Chen, T. Tsai, K. Chang, M. Chen, T. Chang, S. M. Sze, E. T. Yu, J. C. Lee, *Nano Lett.* **2014**, *14*, 813.
- [7] X. Fu, B. Zhang, X. Kang, J. Deng, C. Xiong, T. Dai, X. Jiang, T. Yu, Z. Chen, G. Y. Zhang, *Opt. Express* **2011**, *19*, A1104.

- [8] Y. Jin, F. Yang, Q. Li, Z. Zhu, J. Zhu, S. Fan, *Opt. Express* **2012**, *20*, 15818.
- [9] C. Huh, K. Kim, B. K. Kim, W. Kim, H. Ko, C. Choi, G. Y. Sung, *Adv. Mater.* **2010**, *22*, 5058.
- [10] C. Lin, C. Chen, D. Yeh, C. Yang, *IEEE Photonic Technol. Lett.* **2010**, *22*, 640.
- [11] H. K. Cho, J. Jang, J. H. Choi, J. Choi, J. Kim, J. S. Lee, B. Lee, Y. H. Choe, K. D. Lee, S. H. Kim, K. Lee, S. K. Kim, Y. H. Lee, *Opt. Express* **2006**, *14*, 8654.
- [12] E. Rangel, E. Matioli, Y. Choi, C. Weisbuch, J. S. Speck, E. L. Hu, *Appl. Phys. Lett.* **2011**, *98*, 81104.
- [13] Y. Jin, Q. Li, G. Li, M. Chen, J. Liu, Y. Zou, K. Jiang, S. Fan, *Nanoscale Res. Lett.* **2014**, *9*, 7.
- [14] C. Cho, S. Lee, J. Song, S. Hong, S. Lee, Y. Cho, S. Park, *Appl. Phys. Lett.* **2011**, *98*, 51106.
- [15] M. Kwon, J. Kim, S. Park, *J. Cryst. Growth* **2013**, *370*, 124.
- [16] J. Sung, B. Kim, C. Choi, M. Lee, S. Lee, S. Park, E. Lee, O. Beom-Hoan, *Microelectron. Eng.* **2009**, *86*, 1120.
- [17] K. Jiang, Q. Li, S. Fan, *Nature* **2002**, *419*, 801.
- [18] P. Liu, L. Liu, Y. Wei, K. Liu, Z. Chen, K. Jiang, Q. Li, S. Fan, *Adv. Mater.* **2009**, *21*, 3563.
- [19] S. Luo, K. Wang, J. Wang, K. Jiang, Q. Li, S. Fan, *Adv. Mater.* **2012**, *24*, 2294.
- [20] W. S. Yun, J. Kim, K. Park, J. S. Ha, Y. Ko, K. Park, S. K. Kim, Y. Doh, H. Lee, J. Salvetat, L. Forró, *J. Vacuum Sci. Technol. A* **2000**, *18*, 1329.

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